

DATA SHEET

74ABT534A

Octal D-type flip-flop, inverting
(3-State)

Product specification

1997 Feb 03

IC23 Data Handbook

Octal D-type flip-flop, inverting (3-State)

74ABT534A

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT534A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT534A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the clock operation.

When \overline{OE} is Low, the stored data appears at the outputs. When \overline{OE} is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

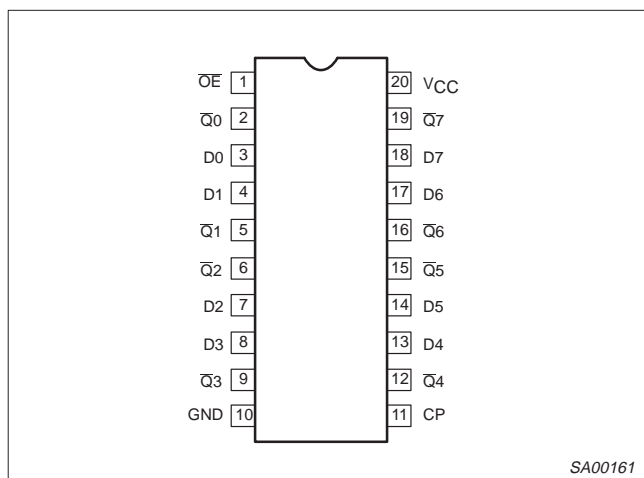
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$ | TYPICAL | UNIT |
|------------------------|---|--|------------|---------------|
| t_{PLH} t_{PHL} | Propagation delay CP to \overline{Q}_n | $C_L = 50\text{pF}; V_{CC} = 5\text{V}$ | 3.3 3.6 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or V_{CC} | 3.5 | pF |
| C_{OUT} | Output capacitance | Outputs disabled; $V_O = 0\text{V}$ or V_{CC} | 6.5 | pF |
| I_{CCZ} | Total supply current | Outputs disabled; $V_{CC} = 5.5\text{V}$ | 100 | μA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|-------------------|-----------------------|----------------|------------|
| 20-Pin Plastic DIP | −40°C to +85°C | 74ABT534A N | 74ABT534A N | SOT146-1 |
| 20-Pin plastic SO | −40°C to +85°C | 74ABT534A D | 74ABT534A D | SOT163-1 |
| 20-Pin Plastic SSOP Type II | −40°C to +85°C | 74ABT534A DB | 74ABT534A DB | SOT339-1 |
| 20-Pin Plastic TSSOP Type I | −40°C to +85°C | 74ABT534A PW | 74ABT534APW DH | SOT360-1 |

PIN CONFIGURATION



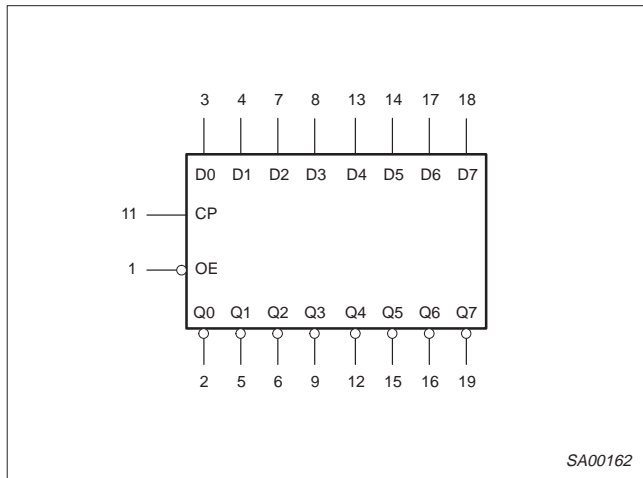
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|-------------------------------|-------------------------------|---|
| 1 | \overline{OE} | Output enable input (active-Low) |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0-D7 | Data inputs |
| 2, 5, 6, 9, 12, 15, 16, 19 | $\overline{Q}0-\overline{Q}7$ | Inverting 3-State outputs |
| 11 | CP | Clock pulse input (active rising edge) |
| 10 | GND | Ground (0V) |
| 20 | V_{CC} | Positive supply voltage |

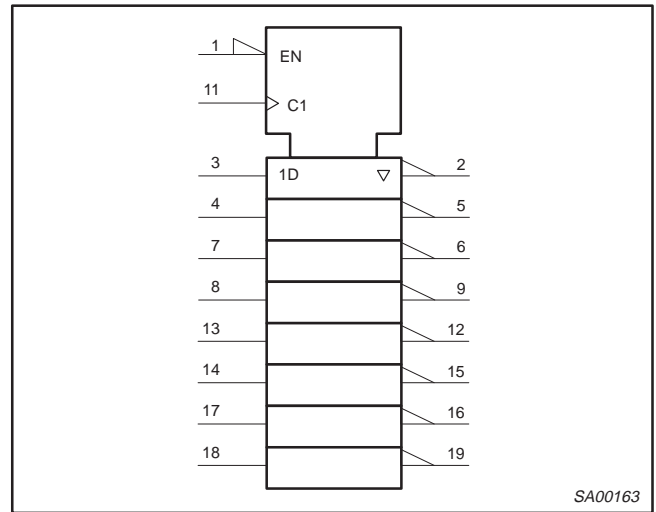
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

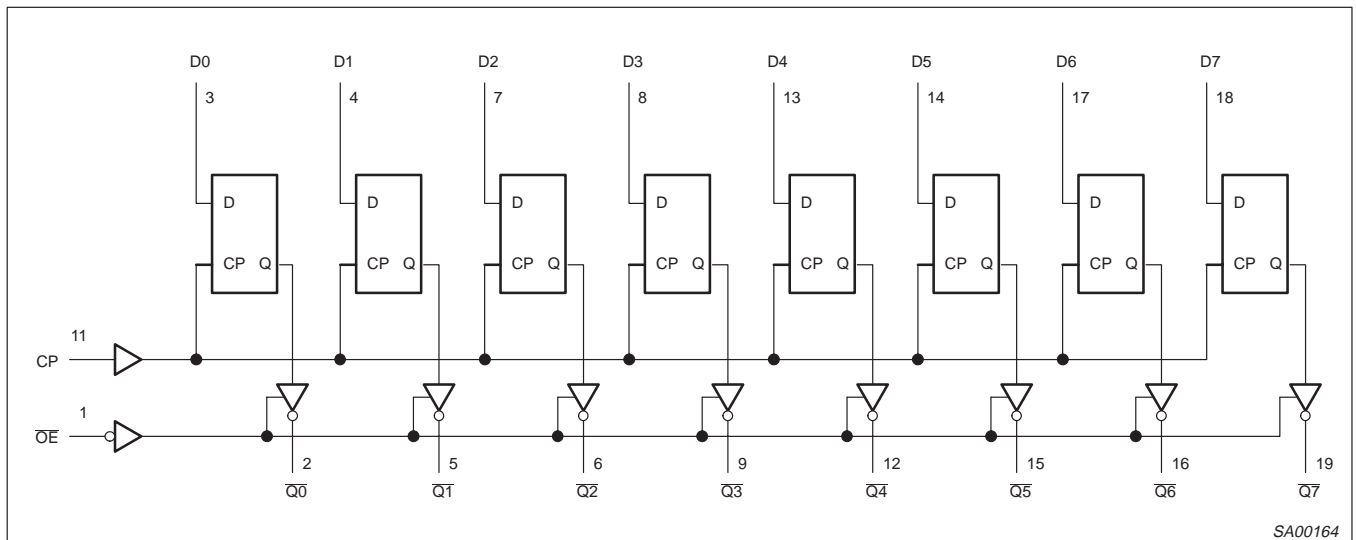


FUNCTION TABLE

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODE |
|-----------------|----------------|----|-------------------|---------------------------------|-------------------------|
| \overline{OE} | CP | Dn | | $\overline{Q0 - \overline{Q7}}$ | |
| L | \uparrow | l | L | H | Latch and read register |
| L | \uparrow | h | H | L | |
| L | \updownarrow | X | NC | NC | Hold |
| H | \updownarrow | X | NC | Z | Disable outputs |
| H | \uparrow | Dn | Dn | Z | |

- H = High voltage level
- h = High voltage level one set-up time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Low-to-High clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- \uparrow = Low-to-High clock transition
- \updownarrow = not a Low-to-High clock transition

LOGIC DIAGRAM



Octal D-type flip-flop, inverting (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I _{IK} | DC input diode current | V _I < 0 | -18 | mA |
| V _I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | -50 | mA |
| V _{OUT} | DC output voltage ³ | output in Off or High state | -0.5 to +5.5 | V |
| I _{OUT} | DC output current | output in Low state | 128 | mA |
| T _{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--------------------------------------|--------|-----------------|------|
| | | Min | Max | |
| V _{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _{IH} | High-level input voltage | 2.0 | | V |
| V _{IL} | Low-level Input voltage | | 0.8 | V |
| I _{OH} | High-level output current | | -32 | mA |
| I _{OL} | Low-level output current | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | 0 | 5 | ns/V |
| T _{amb} | Operating free-air temperature range | -40 | +85 | °C |

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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|----------------------------------|--|--|--------------------------|-------|------|-----------------------------------|------|------|
| | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | |
| | | | Min | Typ | Max | Min | Max | |
| V _{IK} | Input clamp voltage | V _{CC} = 4.5V; I _{IK} = -18mA | | -0.9 | -1.2 | | -1.2 | V |
| V _{OH} | High-level output voltage | V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | 2.5 | 2.9 | | 2.5 | | V |
| | | V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | 3.0 | 3.4 | | 3.0 | | V |
| | | V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH} | 2.0 | 2.4 | | 2.0 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH} | | 0.42 | 0.55 | | 0.55 | V |
| I _I | Input leakage current | V _{CC} = 5.5V; V _I = GND or 5.5V | | ±0.01 | ±1.0 | | ±1.0 | µA |
| I _{OFF} | Power-off leakage current | V _{CC} = 0.0V; V _I or V _O ≤ 4.5V | | ±5.0 | ±100 | | ±100 | µA |
| I _{PU} /I _{PD} | Power-up/down 3-State output current ³ | V _{CC} = 2.0V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = V _{CC} | | ±5.0 | ±50 | | ±50 | µA |
| I _{OZH} | 3-State output High current | V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH} | | 0.1 | 10 | | 10 | µA |
| I _{OZL} | 3-State output Low current | V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH} | | -0.1 | -10 | | -10 | µA |
| I _{CEX} | Output High leakage current | V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC} | | 0.1 | 50 | | 50 | µA |
| I _O | Output current ¹ | V _{CC} = 5.5V; V _O = 2.5V | -50 | -100 | -180 | -50 | -180 | mA |
| I _{CCH} | Quiescent supply current | V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC} | | 100 | 250 | | 250 | µA |
| I _{CCL} | | V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC} | | 24 | 30 | | 30 | mA |
| I _{CCZ} | | V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC} | | 100 | 250 | | 250 | µA |
| ΔI _{CC} | Additional supply current per input pin ² | V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND | | 0.5 | 1.5 | | 1.5 | mA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|--------------------------------------|--|----------|---|------------|--------------------------------------|--|--------------------------------------|------|
| | | | T _{amb} = +25°C V _{CC} = +5.0V | | | T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V | | |
| | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum clock frequency | 1 | 125 | 350 | | 125 | | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to Q _n | 1 | 2.0 ¹ 2.4 ¹ | 3.3 3.6 | 4.2 ¹ 4.7 ¹ | 2.0 2.4 | 5.0 ¹ 5.1 ¹ | ns |
| t _{PZH} t _{PZL} | Output enable time to High and Low level | 3 4 | 1.0 2.6 | 3.1 3.9 | 4.2 4.9 ¹ | 1.0 2.6 | 5.0 5.5 ¹ | ns |
| t _{PHZ} t _{PLZ} | Output disable time from High and Low level | 3 4 | 1.8 ¹ 1.6 ¹ | 3.3 2.8 | 4.3 ¹ 3.6 ¹ | 1.8 ¹ 1.6 ¹ | 4.6 ¹ 4.1 ¹ | ns |

NOTE:

- This datasheet limit may vary among suppliers.

Octal D-type flip-flop, inverting (3-State)

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AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

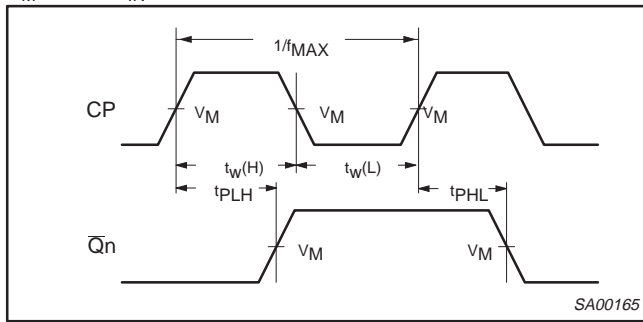
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|--------------------------|-------------------------------------|----------|--|--------------|--|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ | | $T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ | |
| | | | Min | Typ | Min | |
| $t_{s(H)}$ $t_{s(L)}$ | Setup time, High or Low Dn to CP | 2 | 1.0 ¹ 1.0 ¹ | 0.4 0.3 | 1.0 ¹ 1.0 ¹ | ns |
| $t_{h(H)}$ $t_{h(L)}$ | Hold time, High or Low Dn to CP | 2 | 0.5 0.5 | -0.3 -0.4 | 0.5 0.5 | ns |
| $t_w(H)$ $t_w(L)$ | CP pulse width High or Low | 1 | 1.5 ¹ 2.0 ¹ | 0.8 1.0 | 1.5 ¹ 2.0 ¹ | ns |

NOTE:

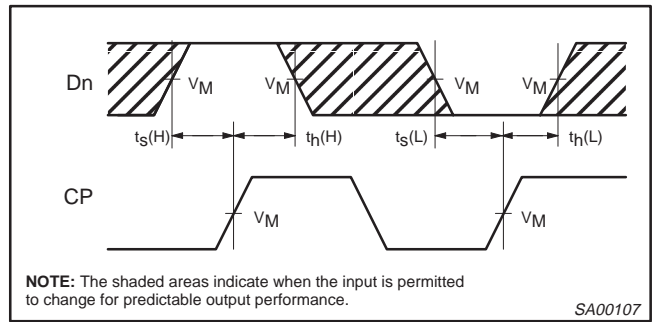
1. This datasheet limit may vary among suppliers.

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$

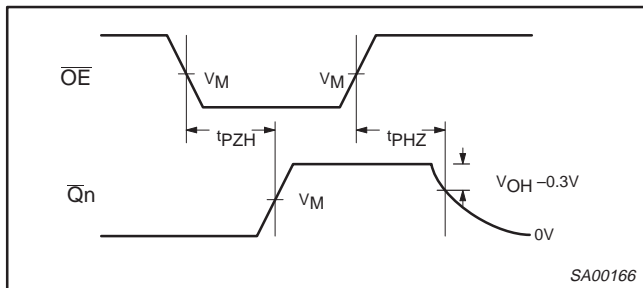


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

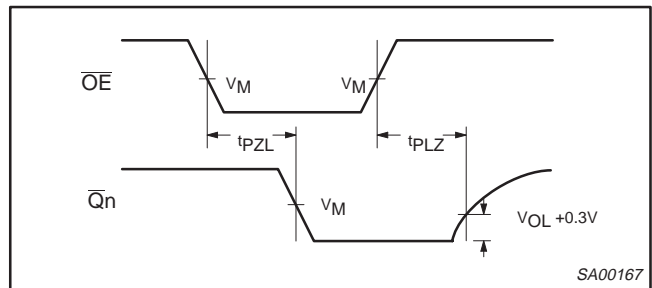


NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2. Data Setup and Hold Times



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

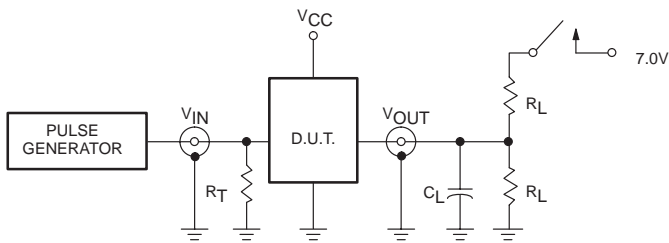


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

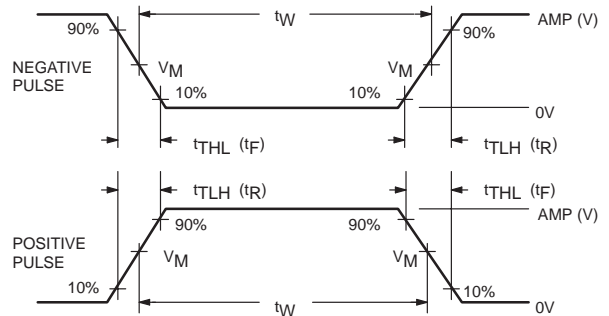
Octal D-type flip-flop, inverting (3-State)

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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$

Input Pulse Definition

SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| t_{PLZ} | closed |
| t_{PZL} | closed |
| All other | open |

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|-------|-------|-------|
| | Amplitude | Rep. Rate | t_W | t_R | t_F |
| 74ABT | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

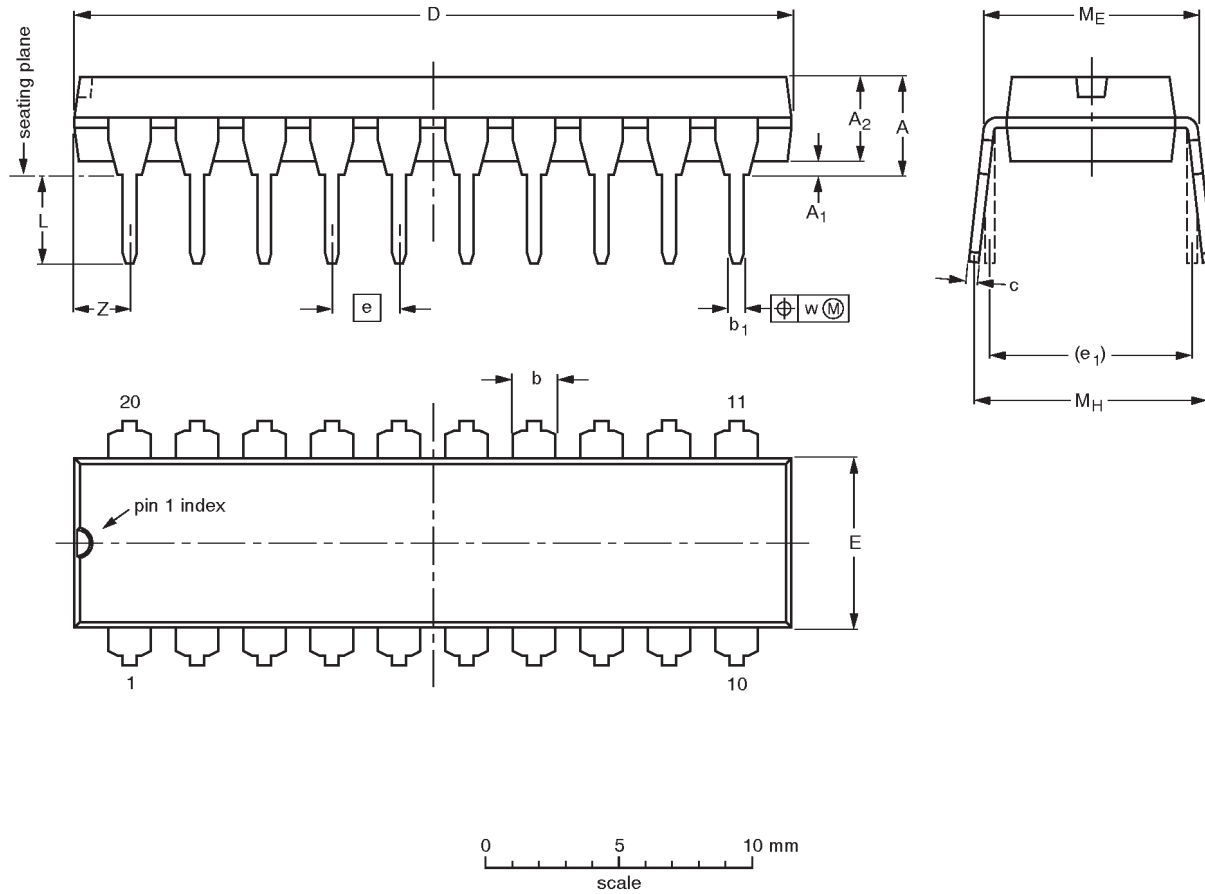
SA00012

Octal D-type flip-flop, inverting (3-State)

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 0.36 0.23 | 26.92 26.54 | 6.40 6.22 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.0 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.014 0.009 | 1.060 1.045 | 0.25 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.078 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

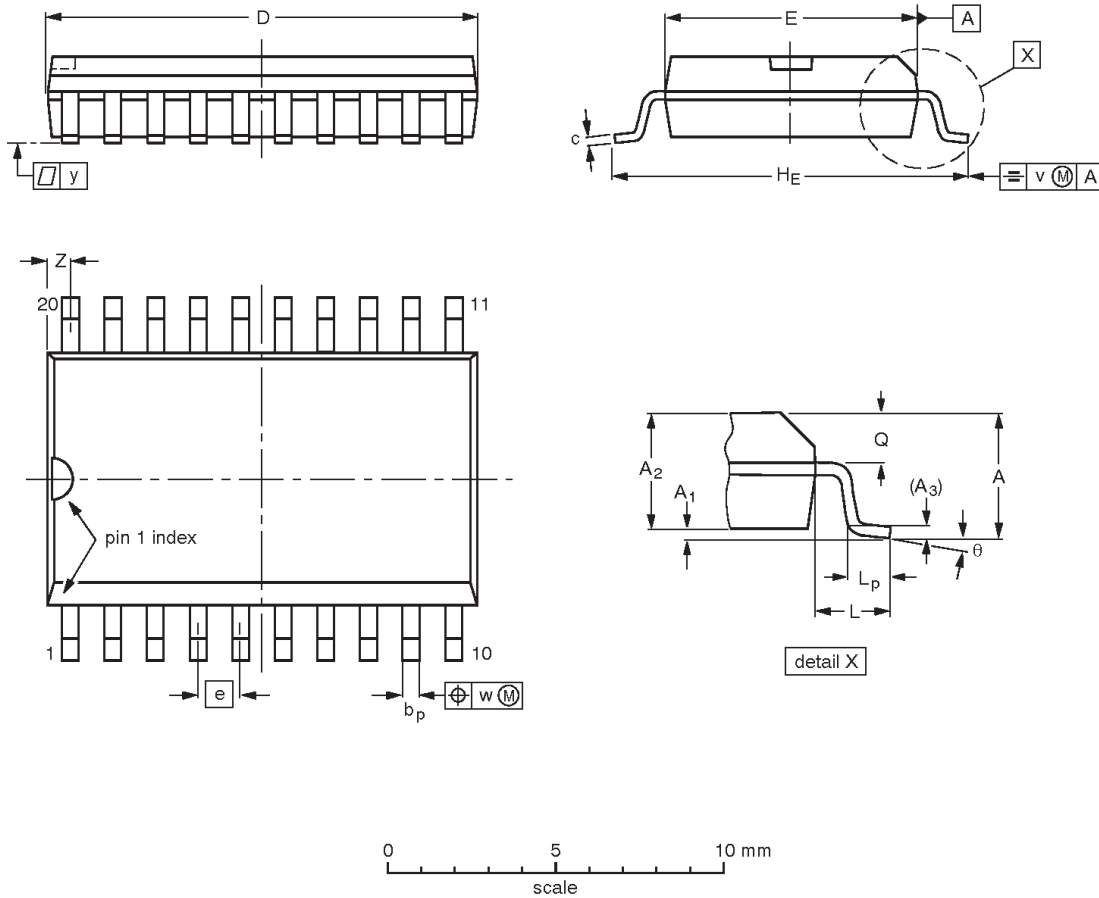
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT146-1 | | | SC603 | | | 92-11-17 95-05-24 |

Octal D-type flip-flop, inverting (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 13.0 12.6 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.51 0.49 | 0.30 0.29 | 0.050 | 0.42 0.39 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | 92-11-17 95-01-24 |

Octal D-type flip-flop, inverting (3-State)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 7.4 7.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 0.9 0.5 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

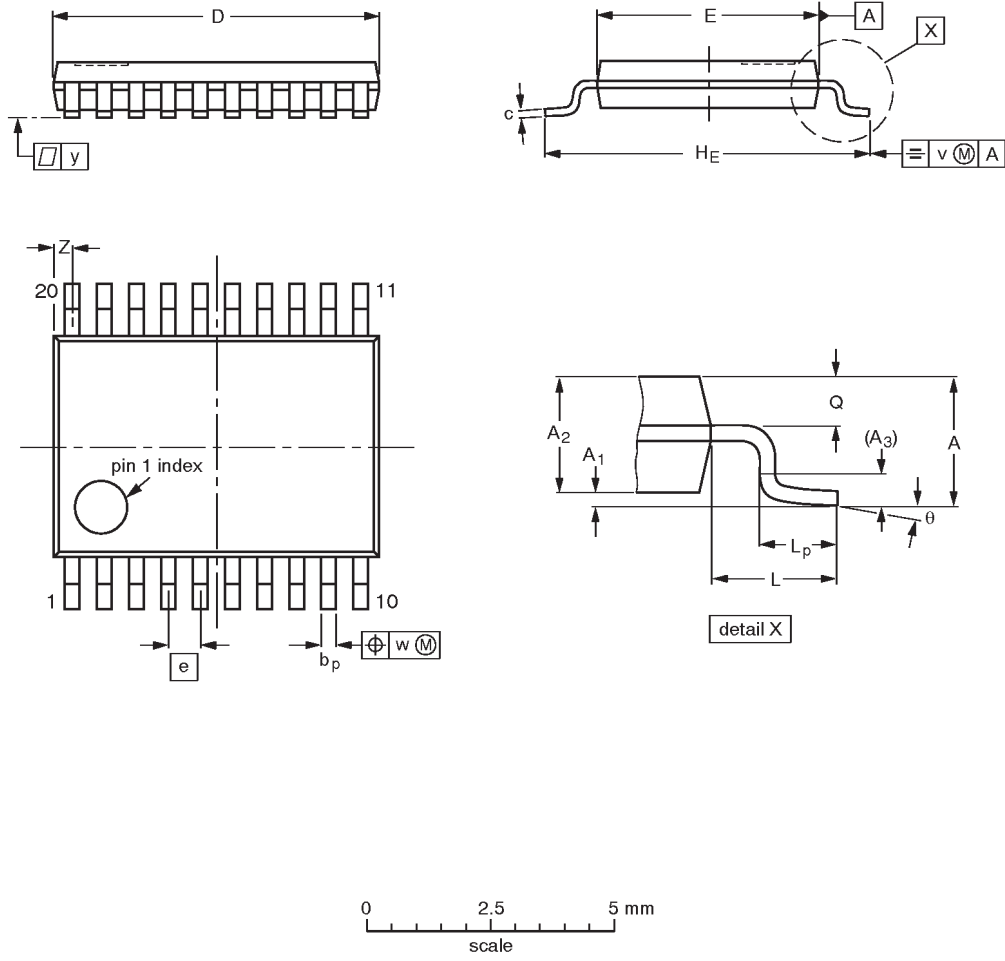
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT339-1 | | MO-150AE | | | | 93-09-08 95-02-04 |

Octal D-type flip-flop, inverting (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.10 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 6.6 6.4 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.5 0.2 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|------------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT360-1 | | MO-153AC | | | | -93-06-16- 95-02-04 |

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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